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EXAMINER
LE, DUY K

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/062,423	Applicant(s) ARIMURA, KAZUYOSHI	
	Examiner Duy K Le	Art Unit 2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 18-24* is/are rejected.

7)☒ Claim(s) *16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,369,622 (Lim et al.).

As to claim 1, Figure 1 in Lim shows a frequency multiplier (100) (see Col. 2, lines 34-54) comprising:

a phase shift section (121) for generating at least one phase shift signal for a fundamental signal (see Col. 2, lines 45-49 and Col. 3, lines 38-42);

a waveform combining section (141) for generating a combined waveform by combining the fundamental signal with the phase shift signal (see Col. 3, lines 53-56); and

a comparator section (131, 132) for comparing a waveform with a comparison threshold value (see Col. 3, lines 48-61).

However, the Lim reference does not disclose arranging a comparator section after the waveform combining section. The Lim reference teaches or suggests arranging a comparator section after the waveform combining section ("various changes in the details, materials, and arrangements of the parts which have been described and illustrated above in order to explain the nature of this invention may be made by those skilled in the art without departing from the principle and scope of the invention" (Col. 5, lines 57-62). In the Lim reference, the comparators

are used to convert the phase-shifted signals into square-wave pulses before combining them to provide an output clock signal with twice the input clock frequency (Col. 3, lines 48-56). In the applicant specification, the phase-shifted signals are combined and input into a comparator to generate square-wave pulses that is twice the input clock frequency). One can do the arrangement of a comparator section after the waveform combining section without affecting the result of generating square-wave pulses that is twice the input clock frequency.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the frequency multiplier of Lim to arrange a comparator section after the waveform combining section, as taught by Lim, in order to have various arrangement of the parts without affecting the result of the multiplier.

As to claim 2, the Lim reference discloses the frequency multiplier according to claim 1, further comprising a level shift section for shifting amplitude levels of at least any one of the fundamental signal and the phase shift signal prior to the generation of the combined waveform (see Col. 3, lines 33-35).

As to claim 3, the Lim reference discloses the frequency multiplier according to claim 1, wherein the phase shift section comprises a phase inverting section (see Col. 2, lines 45-49 and Col. 3, lines 38-42).

As to claim 4, the Lim reference discloses the frequency multiplier according to claim 3, wherein the phase inverting section comprises a differential pair (see Col. 2, lines 45-49 and Col. 3, lines 38-42).

As to claim 5, the Lim reference discloses the frequency multiplier according to claim 1, wherein the phase shift section comprises at least one of a phase advancing section and a phase

delaying section for generating the phase shift signal having a prescribed phase difference with respect to the fundamental signal (see Col. 2, lines 45-54 and Col. 3, lines 38-42).

As to claim 6, the Lim reference discloses the frequency multiplier according to claim 5, wherein the at least one of the phase advancing section and the phase delaying section comprises one of a capacitive load element and an inductive load element (see Col. 2, lines 45-54).

As to claim 7, the Lim reference discloses the frequency multiplier according to claim 1, wherein the comparator section can adjust the comparison threshold value as appropriate (see Col. 3, line 57 to Col. 4, line 5).

As to claim 8, the Lim reference discloses the frequency multiplier according to claim 2, wherein the level shift section can adjust the amplitude levels as appropriate for each of the fundamental signal and the phase shift signal (see Col. 3, lines 33-35).

As to claim 9, the Lim reference discloses the frequency multiplier according to claim 2, wherein the level shift section comprises a switching control section for switching, as appropriate, driving ability for each of the fundamental signal and the phase shift signal (see Col. 5, lines 5-22, 41-49, and Figure 3).

As to claim 10, the Lim reference discloses the frequency multiplier according to claim 9, wherein the driving ability is a size of a transistor for outputting the fundamental signal or the phase shift signal (see Col. 5, lines 32-40).

As to claim 11, the Lim reference discloses the frequency multiplier according to claim 9, wherein the driving ability is a current value of a driving current source for outputting the fundamental signal or the phase shift signal (see Col. 5, lines 32-40).

As to claim 12, the Lim reference discloses the frequency multiplier according to claim 9, wherein the driving ability is a size of a load element for determining a voltage level of the fundamental signal or the phase shift signal (see Col. 5, lines 32-40).

3. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,369,622 (Lim et al.) in view of Emberty et al. (U.S. Patent 6,545,481).

As to claim 13, the Lim reference discloses the frequency multiplier according to claim 1. However, it does not disclose the waveform combining section comprises a rectifier section. The Emberty reference teaches the waveform combining section comprises a rectifier section (see Col. 3, lines 62-65 and Figure 3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the frequency multiplier of Lim wherein the waveform combining section comprises a rectifier section, as taught by Emberty, in order to generate a rectified signal.

As to claim 14, Lim-Emberty discloses the frequency multiplier according to claim 13, wherein the rectifier section comprises a full-wave rectifier section (Emberty: see Col. 3, lines 62-65 and Figure 3).

4. Claims 15 and 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,369,622 (Lim et al.) in view of Otaka (U.S. Patent 6,100,731) and further in view of Emberty et al. (U.S. Patent 6,545,481).

As to claim 15, the Lim reference discloses the frequency multiplier according to claim 1, comprising a first level shift section for biasing an input terminal by proper DC voltages (see Col. 4, lines 3-7 and Figure 2). However, it does not disclose an input differential pair for

receiving the fundamental signal at at least one of differential input terminals thereof, and for outputting differential output signals; a first level shift section for biasing the differential input terminals by proper DC voltages, respectively; a full-wave rectifier section for full-wave-rectifying the differential output signals; and a first comparator section for comparing a full-wave-rectified signal that is output from the full-wave rectifier section with a reference voltage as the comparison threshold value.

The Otaka reference teaches an input differential pair for receiving the fundamental signal at at least one of differential input terminals thereof, and for outputting differential output signals, and a first level shift section for biasing the differential input terminals by proper DC voltages, respectively (see Col. 5, line 64 to Col. 6, line 43 and Figures 7-8).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the frequency multiplier of Lim to further comprise an input differential pair for receiving the fundamental signal at at least one of differential input terminals thereof, and for outputting differential output signals, and a first level shift section for biasing the differential input terminals by proper DC voltages, respectively, as taught by Otaka, in order to support and be able to level shift differential input signals.

However, Lim-Otaka does not disclose a full-wave rectifier section for full-wave-rectifying the differential output signals, and a first comparator section for comparing a full-wave-rectified signal that is output from the full-wave rectifier section with a reference voltage as the comparison threshold value. The Emberty reference teaches a full-wave rectifier section for full-wave-rectifying the differential output signals (see Col. 3, lines 62-65 and Figure 3), and a first comparator section for comparing a full-wave-rectified signal that is output from the full-

wave rectifier section with a reference voltage as the comparison threshold value (see Col. 4, lines 10-11 and Figure 3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the frequency multiplier of Lim-Otaka to further comprise a full-wave rectifier section for full-wave-rectifying the differential output signals, and a first comparator section for comparing a full-wave-rectified signal that is output from the full-wave rectifier section with a reference voltage as the comparison threshold value, as taught by Emberty, in order to provide a threshold detection.

As to claim 18, Lim-Otaka-Emberty discloses the frequency multiplier according to claim 15, further comprising: two or more input differential pairs for receiving the fundamental signal and the at least one phase shift signal having the prescribed phase difference with respect to the fundamental signal (Otaka: see Col. 5, line 64 to Col. 6, line 23 and Figure 7); and one of a phase advancing section and a phase delaying section for generating each phase shift signal individually (Otaka: see Col. 3, lines 41-50).

As to claim 19, Lim-Otaka-Emberty discloses the frequency multiplier according to claim 15, wherein the first level shift section further comprises a switching control section for switching, as appropriate, sizes of transistors of a transistor pair of the input differential pair or resistance values of load resistors of the input differential pair (Otaka: see Col. 5, line 64 to Col. 6, line 43 and Figures 7-8).

As to claim 20, Lim-Otaka-Emberty discloses the frequency multiplier according to claim 15, wherein load resistors that are connected to the input differential pair are active loads including MOS transistors (Otaka: see Col. 6, lines 1-14 and Col. 7, lines 13-15), and the first

level shift section further comprises a switching control section for switching and controlling bias voltages for gate terminals of the respective MOS transistors (Otaka: see Col. 6, lines 24-27 and Figures 7-8).

As to claim 21, Lim-Otaka-Emberty discloses the frequency multiplier according to claim 15, wherein load resistors that are connected to the input differential pair are active loads including bipolar transistors (Otaka: see Col. 6, lines 1-14 and Col. 7, lines 13-15), and the first level shift section comprises a switching control section for switching and controlling base currents flowing through base terminals of the respective bipolar transistors (Otaka: see Col. 6, lines 24-27 and Figures 7-8).

As to claim 22, Lim-Otaka-Emberty discloses the frequency multiplier according to claim 18, wherein the first level shift section comprises a switching control section for switching and controlling current values of bias current sources for driving the input differential pairs (Otaka: see Col. 5, line 64 to Col. 6, line 43 and Figures 7-8).

5. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,369,622 (Lim et al.) in view of Takahashi (U.S. Patent 6,072,374).

As to claim 23, the Lim reference discloses the frequency multiplier according to claim 1. However, it does not disclose an FM modulator, wherein the fundamental signal is obtained by frequency-modulating an original signal with the FM modulator when the original signal is a frequency signal. The Takahashi reference teaches an FM modulator, wherein the fundamental signal is obtained by frequency-modulating an original signal with the FM modulator when the original signal is a frequency signal (see Col. 2, lines 48-61 and Figures 1-3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the frequency multiplier of Lim to further comprise an FM modulator, wherein the fundamental signal is obtained by frequency-modulating an original signal with the FM modulator when the original signal is a frequency signal, as taught by Takahashi, in order to generate a FM modulated signal.

6. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,369,622 (Lim et al.) in view of Dougherty (U.S. Patent 4,658,323).

As to claim 24, the Lim reference discloses the frequency multiplier according to claim 1. However, it does not disclose a V/F converter, wherein the fundamental signal is a frequency signal obtained by converting an original signal with the V/F converter when the original signal is a voltage signal. The Dougherty reference teaches a V/F converter, wherein the fundamental signal is a frequency signal obtained by converting an original signal with the V/F converter when the original signal is a voltage signal (see Col. 2, lines 32-38, Col. 5, lines 48-52, Figures 1 and 7).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the frequency multiplier of Lim to further comprise a V/F converter, wherein the fundamental signal is a frequency signal obtained by converting an original signal with the V/F converter when the original signal is a voltage signal, as taught by Dougherty, in order to convert a voltage analog signal into a frequency.

Allowable Subject Matter

7. Claims 16-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As to claims 16 and 17, the prior art of record fails to show or fairly suggest high-pass filter sections provided for the respective differential output terminals, for interrupting DC components that are output from the respective differential output terminals; a second level shift section for biasing differential signals that are output from the high-pass filter sections by proper DC voltages, respectively, in combination with other features cited in the claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Laws (U.S. Patent 6,664,824) discloses frequency doubler circuit arrangement.

b. Hirata (U.S. Patent 5,703,509) discloses frequency multiplier circuit.

c. McGuffin et al. (U.S. Patent 3,922,593) discloses circuit for producing odd frequency multiple of an input signal.

d. Riley (U.S. Patent 4,691,170) discloses frequency multiplier circuit.

e. Choi (U.S. Patent 5,166,836) discloses digital signal detecting apparatus.

f. Fujii et al. (U.S. Patent 5,708,399) discloses modulator and frequency multiplier for use therein.

g. Besson et al. (U.S. Patent 5,194,820) discloses frequency doubling device.

h. Nakajima (U.S. Patent 6,456,836) discloses frequency multiplier and wireless device incorporating same.

i. Francis (U.S. Patent 6,564,045) discloses broadband frequency multiplier.

j. Zhang et al. (U.S. Patent 5,815,014) discloses transistor based frequency multiplier.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duy K Le whose telephone number is 703-305-5660. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward F Urban can be reached on 703-305-4385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Duy Le
July 9, 2004

7/12/04

QUOCHIEN B. VUONG
PRIMARY EXAMINER